REV	DESCRIPTION	DATE	BY
A13	OFFICIAL RELEASE VERSION	10/11/2017	Han

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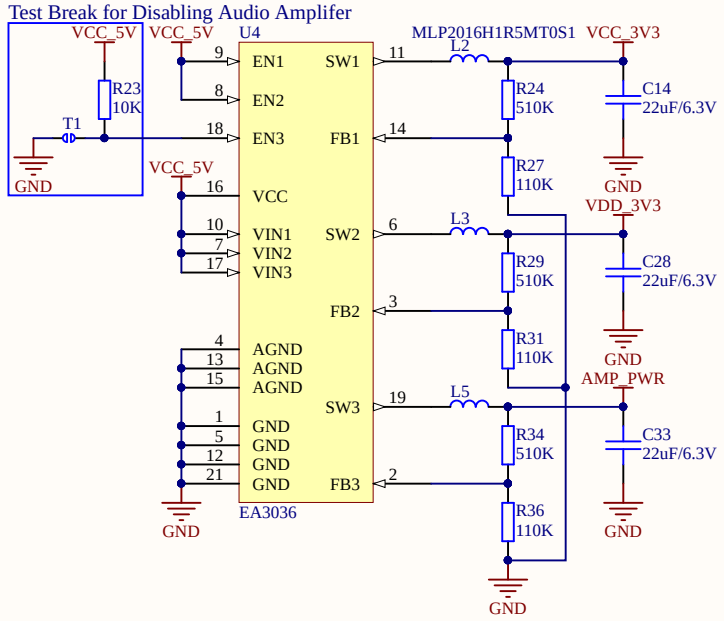
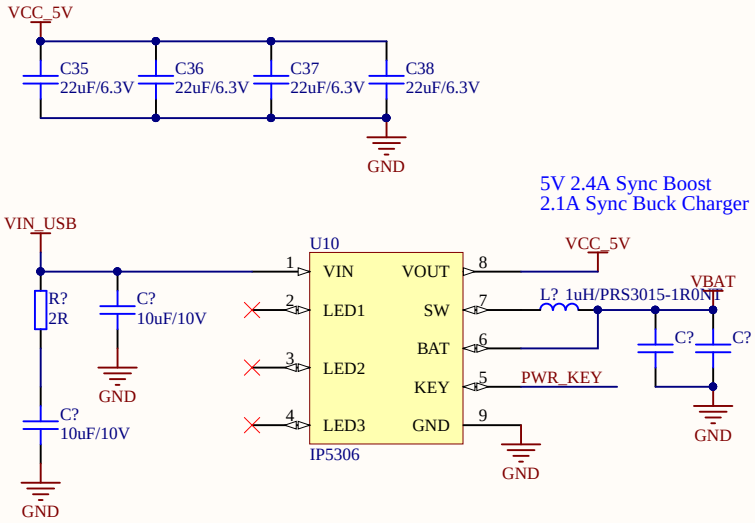
M5 STACK M5 STACK CORE

Title: M5 STACK CORE COVER

Size	Number	Revision
A4	013-0000-001	A

Date:	2017/12/6	Sheet	of
File:	C:\Users\..\A1-COVER.SchDoc	Drawn By:	Han Shihao





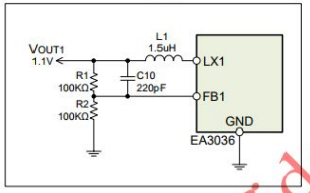
Link for Datasheet: http://198.13.102.98/bj/ingenic_support/X1000_X1000E_X1500/02_HW/00_Halley2/Halley2_coreV3.0_baseV2.0/06Datasheet/PMIC/EA3036_1.0_2014_Sep.pdf

Application Information

Output Voltage Setting

Each of the regulators output voltage can be set via a resistor divider (ex. R1, R2). The output voltage is calculated by following equation:

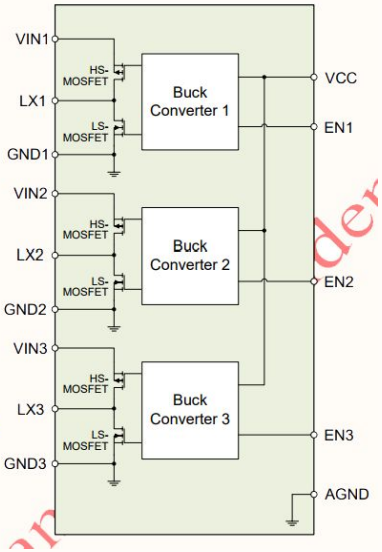
$$V_{OUT1} = 0.6 \times \frac{R1}{R2} + 0.6\ V$$



The following table lists common output voltage and the corresponding R1, R2 resistance value for reference.

Output Voltage	R1 Resistance	R2 Resistance	Tolerance
3.3V	510KΩ	110KΩ	1%
1.8V	200KΩ	100KΩ	1%
1.5V	150KΩ	100KΩ	1%
1.2V	100KΩ	100KΩ	1%

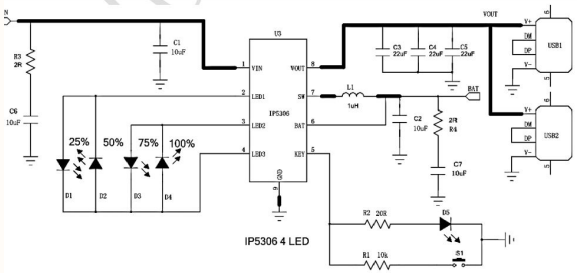
Function Block Diagram



Link for DCDC Buck Inductor: http://www.mouser.com/ds/2/400/nductor_commercial_power_mlp2016_en-838407.pdf

Type		Thickness T (mm)max.	L (μH)	tolerance	Measuring frequency (MHz)	DC resistance (Ω)	Rated current* (mA)max.	Part No.
Low core loss	Low resistance	1.0	0.47	±20%	2	0.055±25%	1700	MLP2016HF47MT0S1
		1.0	1.0	±20%	2	0.09±25%	1300	MLP2016H1R0MT0S1
		1.0	1.5	±20%	2	0.11±25%	1200	MLP2016H1R5MT0S1
		1.0	2.2	±20%	2	0.11±25%	1200	MLP2016H2R2MT0S1
		1.0	3.3	±20%	2	0.12±25%	1200	MLP2016H3R3MT0S1
		1.0	4.7	±20%	2	0.16±25%	1100	MLP2016H4R7MT0S1
	Emphasized DC bias characteristics	1.0	0.47	±20%	2	0.07±25%	1500	MLP2016VR47MT0S1
		1.0	1.0	±20%	2	0.12±25%	1200	MLP2016V1R0MT0S1
		1.0	1.5	±20%	2	0.14±25%	1150	MLP2016V1R5MT0S1
		1.0	2.2	±20%	2	0.17±25%	1000	MLP2016V2R2MT0S1

Datasheet for IP5306:
http://www.injoinic.com/doc/IP5306%C2%A0datasheet%C2%A0v1.01.pdf



M5 STACK

M5 STACK CORE

Title: M5 STACK CORE POWER MANAGEMENT

Size	Number	Revision
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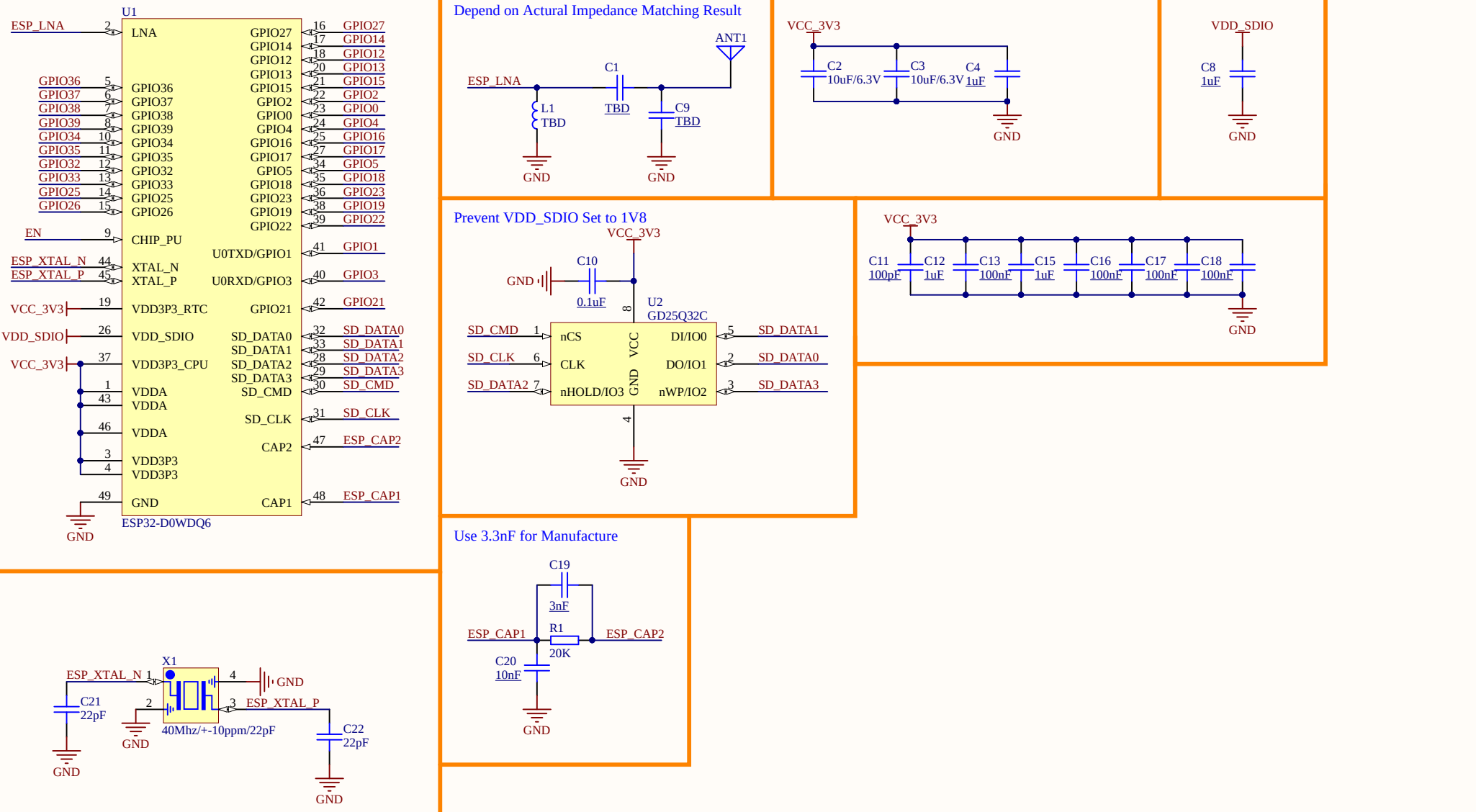
File:	C:\Users\..\A1-PWR.SchDoc	Drawn By:	Han Shihao



M5 STACK CORE		
Title: M5 STACK CORE ESP32 SUBSYSTEM		
Size: A4	Number: 013-0000-003	Revision: A
Date: 2017/12/6	Sheet of	
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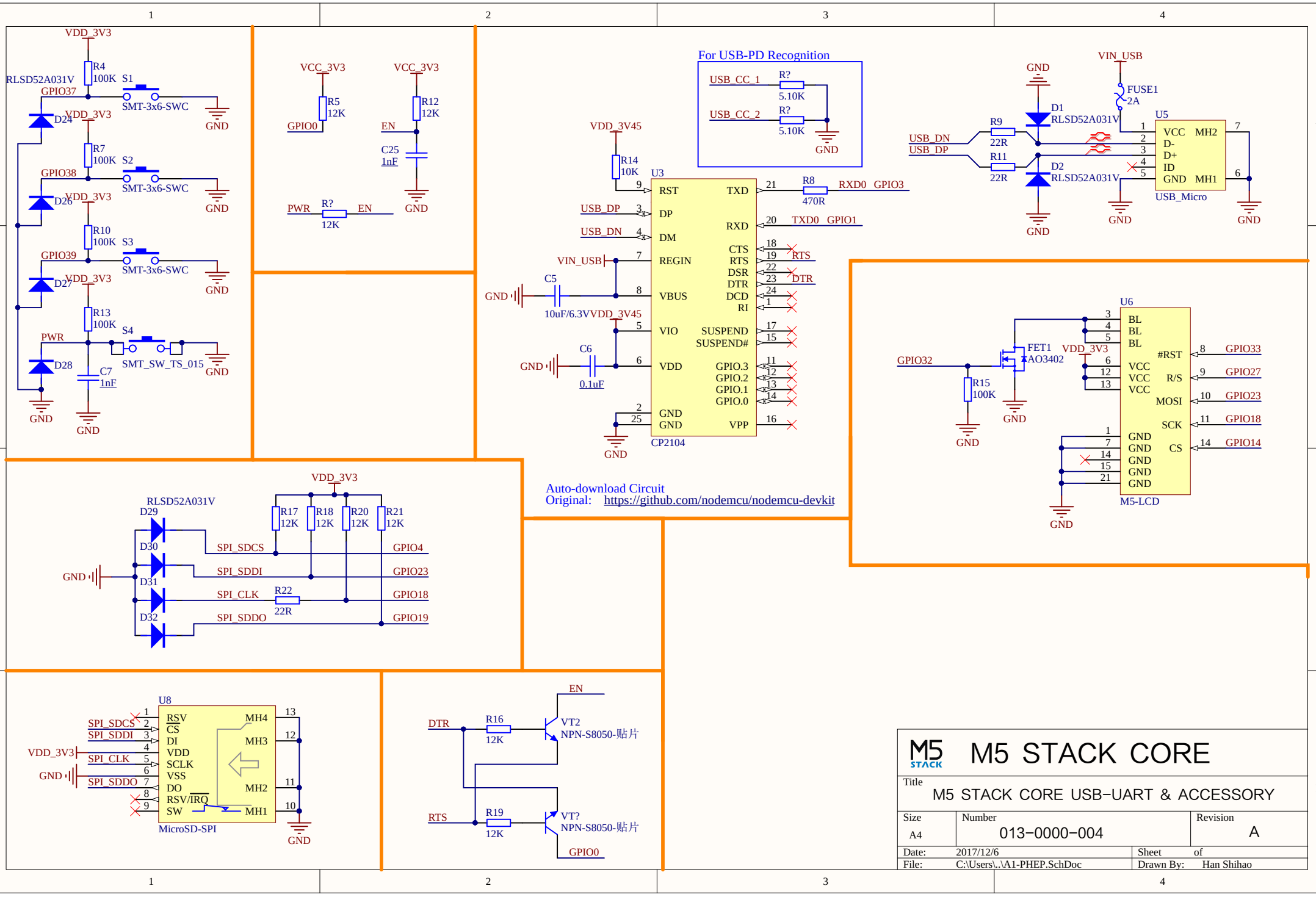

M5 STACK

M5 STACK CORE

Title	M5 STACK CORE USB-UART & ACCESSORY	
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Date: 2017/12/6	Sheet of	
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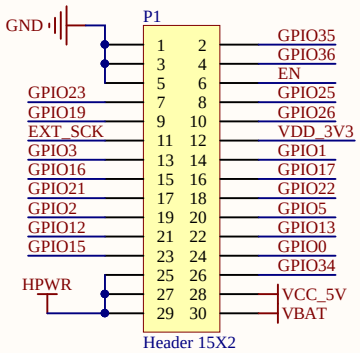
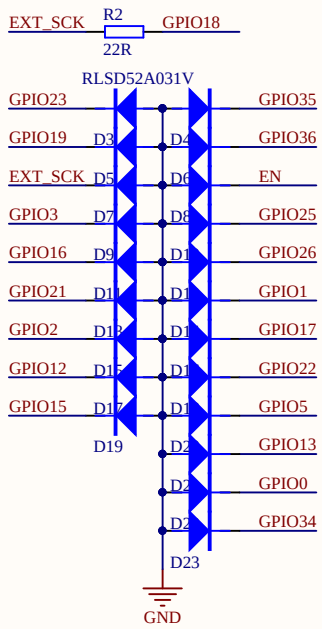




	GND	1	2	ADC1	GPIO35
	GND	3	4	ADC2	GPIO36
	GND	5	6	RESET	EN
GPIO23	MOSI	7	8	DAC0/AUDIO_L	GPIO25
GPIO19	MISO	9	10	DAC1/AUDIO_R	GPIO26
GPIO18	SCK	11	12	3.3V	
GPIO3	IO0/RXD1	13	14	IO1/TXD1	GPIO1
GPIO16	IO2/RXD2	15	16	IO3/TXD2	GPIO17
GPIO21	IO4/SDA	17	18	IO5/SCL	GPIO22
GPIO2	IO6	19	20	IO7	GPIO5
GPIO12	IO8/IIS_SCLK	21	22	IO9/IIS_WS	GPIO13
GPIO15	IO10/IIS_OUT	23	24	IO11/IIS_MCLK/BOOT	GPIO0
	HPWR	25	26	ADC0/IIS_IN	GPIO34
	HPWR	27	28	5V	
	HPWR	29	30	BATTERY	

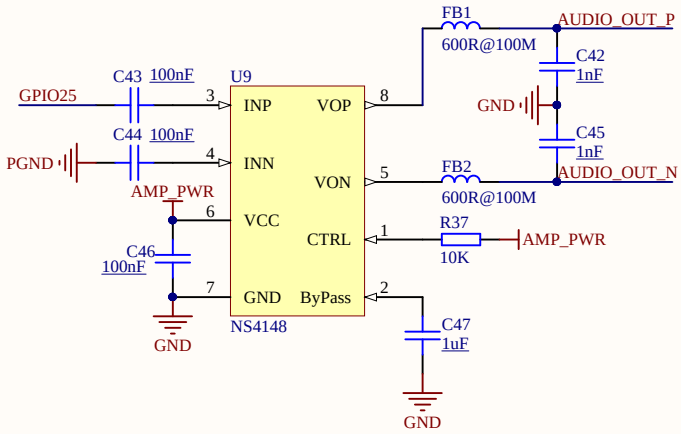
M5 STACK

M5 STACK CORE

Title: M5 STACK CORE M.BUS DEFINATION

Size	Number	Revision
A4	013-0000-005	A

Date:	2017/12/6	Sheet	of
File:	C:\Users\..\A1-MBUS.SchDoc	Drawn By:	Han Shihao



Link for Datasheet: http://www.chipsourcetek.com/Uploads/file/20151207193630_0605.pdf

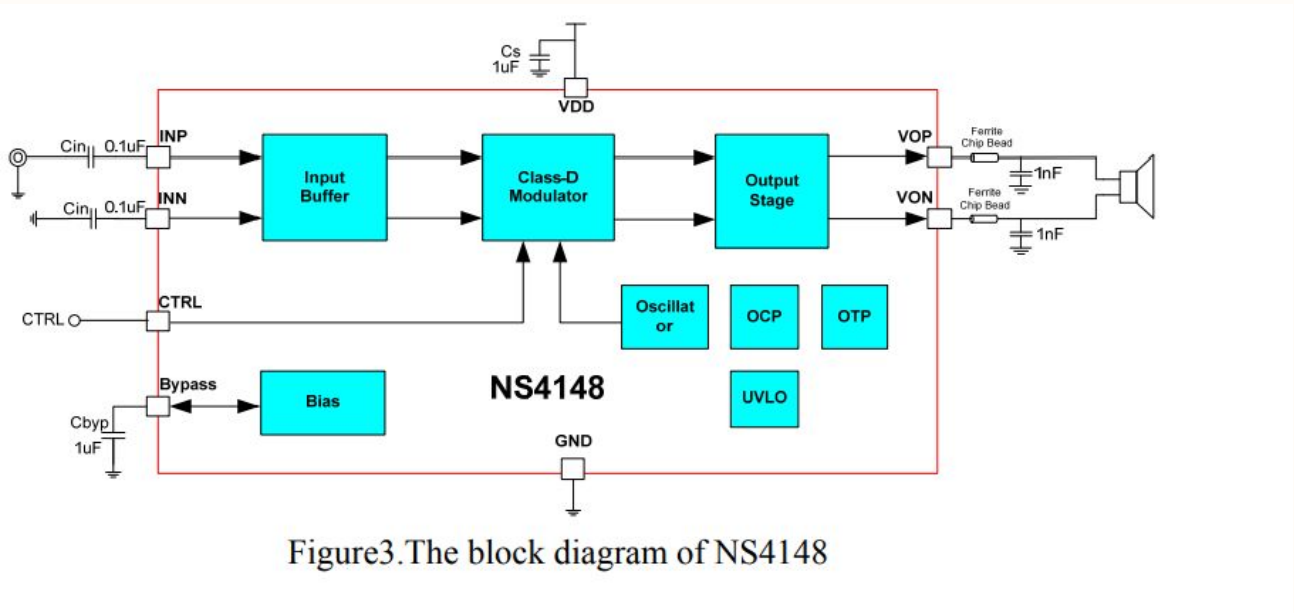


Figure3.The block diagram of NS4148

M5 STACK	M5 STACK CORE	
Title	M5 STACK CORE AUDIO AMPLIFER	
Size: A4	Number: 013-0000-006	Revision: A
Date: 2017/12/6	Sheet of	
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